Instructions: *Use pencil. Multiple-choice questions all count the same. Unless otherwise indicated, each fill-in and short answer question counts the same as one multiple-choice question. Diagrams count the same as two multiple-choice questions. Answer all questions: there is no penalty for guessing.* **No electronic devices of any sort may be used. All phones must be off, not just silent.**

The single-cycle datapath figure is based on the one you used for Assignment 8. Most of the letters, however, are different. Where possible, I put the letters inside the symbols rather than outside them, and several letters are duplicated to make it easier to see what is connected to what. For example, the outputs of the Control (letter **J**) go to 9 different places, and the **J** is repeated at five of them. *After printing the figure, I saw that **F** should also have been a **J**.* There is no significance to these changes; they are simply intended to make the figure easier to work with than the one provided with the homework.

Use the following values for the questions relating to the single-cycle datapath diagram:

Element	Time Delay
Wires; bit concatenation, etc.	0 ps
Individual gates	2 ps
Multiplexers	5 ps
Control logic; ALU control	35 ps
Read a new value from a single register (the PC)	20 ps
Read values from the register file	70 ps
Write a value into the register file	70 ps
32-bit parallel adder	60 ps
ALU	110 ps
Read or write any memory	150 ps

1. For the single-cycle datapath, how soon after the PC is loaded with an address are the values of the control signals, **J**, valid? In this and all questions, show all work for possible partial credit.
    A.   145 ps
    B.   160 ps
    C.   175 ps
    D.   190 ps
    E.   205 ps
2. What instruction format does *not* depend on the time at which point **M** is valid?
    A.   R
    B.   I
    C.   J
    D.   M
    E.   V
3. When do the values of **C** and **D** become valid?

	C	D
A.	80 ps	140 ps
B.	80 ps	150 ps
C.	80 ps	160 ps
D.	80 ps	170 ps
E.	90 ps	150 ps

4. Fill in the values in this table for the instructions indicated. (*Each row counts the same as one multiple-choice question.*)

Instruction	M	N	O	G
R-type				
beq				
lw				

5. For each of the following instructions, tell whether **C**, **E**, or **H** is the critical value for determining when **Q** becomes valid. *Do not try to answer this question until you complete the previous one.*
   A. ____ R-type
   B. ____ *beq*
   C. ____ *lw*

6. What is the relationship between the values of **I** and **D**?
   A. **I** is always 5 ps less than **D**
   B. **I** is always equal to **D**
   C. **I** is always 5 ps greater than **D**
   D. It depends on the format of the instruction
   E. There is no way to tell

7. How long is needed for an *lw* instruction to produce the value that will be written to the register file (**L**)?
   A. 465 ps
   B. 505 ps
   C. 545 ps
   D. 585 ps
   E. 625 ps

8. The reciprocal of 625 is 0.0016. What would be the maximum clock frequency that could be used with the single-cycle datapath if your answer to Question 7 was E? *Adjust the answer so it is a decimal number with an integer part between 1 and 999.* Be sure to use the correct unit of measurement. Answer here: _____.

9. Give the value of *RegDst* (**0** or **1**) for each of the following instructions. Use **X** if the instruction would execute correctly whatever the value of *RegDst* might be.
   A. ____ R-type
   B. ____ *lw*
   C. ____ *sw*
   D. ____ *beq*
   E. ____ *j (jump)*

10. If a single-cycle datapath design has a clock frequency of 500 MHz, what would be the clock speed for a datapath using components with the same speeds, but using a pipelined design with 4 perfectly-balanced stages?
   A. 1.5 GHz
   B. 2.0 GHz
   C. 2.5 GHz
   D. 3.0 GHz
   E. 3.5 GHz

11. A hard disk spins at 7200 RPM. What is its *period*? Using the correct unit of measure counts._____

12. What is the average *rotational delay* for the disk in Question 11? Using the correct unit of measure counts. _____

Questions 13 through 16 are based on the datapaths described in Question 10. **Be sure to give both the numerical value and the proper unit of measure.**

13. What would be the *instruction latency* for the single-cycle design?   _____

14. What would be the instruction latency for the *pipelined design*?   _____

15. What would be the *instruction throughput* for the single-cycle design?   _____

16. What would be the instruction throughput for the *pipelined design*?   _____

Put an X in front of each of the following statements that is *true*. Leave *false* statements blank.

17. ____ *Register forwarding* deals with control hazards by adding stages to the pipeline.

18. ____ *Branch prediction* deals with control hazards by processing instructions before the decision whether execute them or not has been made.

19. ____ Some *structural hazards* can be dealt with by using multiple parallel adders instead of doing all arithmetic in the ALU.

20. ____ *Data hazards* can be dealt with by eliminating conditional branch instructions.

21. ____ *Register forwarding* obtains operands from pipeline registers instead of the register file to deal with data hazards.

22. IF, ID, EXE, MEM, and WB are the names of the stages of the pipelined datapath in chapter 4 of the textbook. How many *pipeline registers* are there?
    A. 0
    B. 1
    C. 2
    D. 4
    E. 32

23. What information is in the IF/ID pipeline register?
    A. Only the instruction
    B. Only PC+4
    C. Both the instruction and PC+4, but nothing else
    D. The instruction, PC+4, and the values of R[rs] and R[rt], but nothing else.
    E. All of the above plus all the control signals.

A computer has 4 GB of byte-addressable primary memory with 4 bytes per word. There is a 4-way set associative cache with a capacity of 256 KB. There are 32 words per cache line.

24. Fill in the following values:

Parameter	Value
Bytes per line	
Number of lines	
Number of sets	
Number of main memory address bits	
Byte offset bits	
Block offset bits	
Index bits	
Tag bits	

26. What is the *average access time* for this memory system if the cache access time is 10 ps, the *miss penalty* is 100 ps (that is, the total access time for a miss is 110 ps), and the probability of a hit is 0.9?
    A. 20 ps
    B. 30 ps
    C. 20 GHz
    D. 30 GHz
    E. 3.14159