NOTE: It is my policy to give a failing grade in the course to any student who either gives or receives aid on any exam or quiz.

INSTRUCTIONS: Circle the letter of the best answer for each multiple choice question. Fill in the blanks where indicated, and draw diagrams either under the questions or on the backs of the exam sheets.

1. Write the truth table for a full adder.

2. Use a Karnaugh Map to minimize the *carry out* (C_{out}) function of a full adder. Write the minimized equation, and show which product term relates to each circle in the Karnaugh Map.

3. Draw a schematic diagram of the leftmost bit of an ALU that can perform the following operations, depending on the values of two inputs named F_1 and F_0:

F_1	F_0	Function
0	0	Add
0	1	Subtract
1	0	OR
1	1	AND

Be sure to include the all logic for generating the Carry, oVerflow, and Negative condition code bits. In addition, show how the logic for generating the Zero bit would be formed. Use symbols for the full adder and the multiplexer(s) instead of drawing all the gates inside them. Label all inputs and outputs.

4. Assume the ALU in Question 3 is four bits wide, and complete the following table to show what it will do. You may omit the C and V values for AND and OR operations.

A	B	F_1	F_0	C_0	Result	CVNZ
0000	0000	0	0	0		
1111	0110	1	1	0		
0110	1111	0	1	1		
1010	1101	0	0	0		

5. Which of the following describes a 8×1 multiplexer?
   A. Three select pins, eight data input pins, and one output pin.
   B. Three data input pins, one select input pin, and eight output pins.
   C. Eight select input pins, one data output pin, and three inverters.
   D. Eight inverters, four input pins, and one output pin.
   E. 32 input pins, 32 output pins, and 32 AND gates.

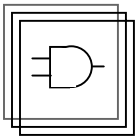
6. Tell how to construct a 8×32 multiplexer. Use sentences, not a diagram.

7. What is the period of a clock with a 4 MHz frequency? Be sure to indicate the correct unit of measure along with your numerical answer. (*e.g., "14 cm" rather than just "14".*) _____

8. Draw any logic network you want that has five gates and three propagation delays:

9. Describe the procedure for converting a schematic diagram into a symbol in Quartus, and explain how the symbol can then be used once it has been created.

10. What is this tool used for in Quartus: (Pick the *best* answer.)



   A. To convert a schematic to Verilog
   B. To insert any component from a library.
   C. To insert an AND gate
   D. To insert an OR gate
   E. To add a wire
   F. To turn on a seven-segment display

11. Each web page a user views requires the browser to send exactly one request to the server, but the server might return multiple files as a result of the request. (*Hint: try a different answer this time.)*
   A. True
   B. False

12. Draw a schematic diagram showing the internal structure (i.e. the gates) of a D flip-flop. Label all inputs and outputs meaningfully.

13. Draw a diagram showing the relationships among the following items in a Finite State Machine (FSM): i.) External Inputs, ii.) Clock input, iii.) External Outputs, iv.) Flip-flops, v.) Combinational Logic, vi.) Present State, vii.) Next State.

14. Tell how the Present State and Next State relate to the D and Q pins of the flip-flops in a FSM. Make sure you explain what are inputs and what are outputs for everything mentioned.

15. What is a *decoder* used for in the design of the MIPS register file?
    A. To select the two registers to read from.
    B. To select the register to write to.
    C. To decode the operation code.
    D. To decode the ALU function code.
    E. To subtract.

16. Tell how many flip-flops are in each of the following items:
    A. One register of the MIPS CPU: _____
    B. The entire MIPS register file: _____
    C. The MIPS ALU: _____
    D. A binary counter with 8 states using an encoded design: _____
    E. A FSM with 8 states using a "one hot" design: _____

17. (a) Draw a state diagram for a 2-bit binary counter that only changes state when its single input, named "up" is true. (b) Draw a complete state table for this machine, labeling each column meaningfully. (c) Convert the state table into a circuit schematic. You may answer on the back of an exam sheet if there is not enough room below, but be sure to write the question number (17) next to your answer if you do.