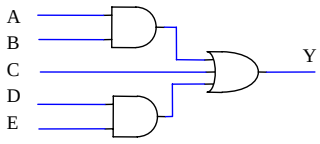
NOTE: It is my policy to give a failing grade in the course to any student who either gives or receives aid on any exam or quiz.

INSTRUCTIONS: Answer multiple choice questions by circling the letter of the single best single answer. Answer other questions as directed. Unless otherwise indicated, all questions count equally.

1. How many propagation delays are there in the following network?



   A. 0
   B. 1
   C. 2
   D. 3
   E. 4

2. How many milliseconds are there in a second?
   A. 0.1
   B. 10
   C. 100
   D. 1,000
   E. 10,000

3. How many picoseconds are there in a microsecond?
   A. 0.001
   B. 1,000
   C. 10,000
   D. 100,000
   E. 1,000,000

4. To convert microseconds to nanoseconds:
   A. Multiply the number of microseconds by 1,000
   B. Multiply the number of microseconds by 1,000,000
   C. Multiply the number of microseconds by 0.001
   D. Multiply the number of microseconds by 0.000001
   E. Take the reciprocal of the number of microseconds.

5. What is the period of a 2 GHz clock?
   A. 2,000,000 seconds
   B. 2,000 picoseconds
   C. 500 picoseconds
   D. 500 nanoseconds
   E. 500 microseconds

6. Not counting the Global Reset button, how many push buttons are there on the UP3 logic board?
   A. 1
   B. 2
   C. 4
   D. 8
   E. 16

7. What has to go between a schematic output wire and an actual output device on the UP3, such as a LED?
   A. A flip-flop
   B. An AND gate
   C. An input pin
   D. An output pin
   E. A Verilog module

8. How do you connect FPGA pins to particular buttons on the UP3 board?
   A. Use the Assignments → Pin Assignments menu.
   B. Use the schematic editor to put the buttons in the circuit diagram.
   C. Write a Verilog statement to connect them.
   D. Quartus takes care of this for you automatically.
   E. It can't be done.

9. Complete the truth table for a full adder:

A_i	B_i	C_{in}	C_{out}	Sum_i
0	0	0		

10. Complete the Karnaugh Map for the C_{out} function, and write the resulting equation below.

B_i C_{in} / A_i	00	01	11	10
0				
1				

C_{out} = _____

11. Draw a complete schematic for one bit slice of the MIPS ALU on the back of this sheet. You may use block symbols for multiplexers and full adders, but draw all the gates for everything else. Label the inputs A_{inv} B_{neg} A_i B_i and C_{in}, and label the outputs R_i and C_{out}.

12. Complete the indicated rows of the truth table for a four-bit version of the MIPS ALU. Note that the 4-bit values for A and B are given in hexadecimal. Use hexadecimal for the Result column. Use binary for all other values. Do not supply values for the blacked-out cells.

A	B	A_{inv}	B_{neg}	F_1	F_0	Result	C	V	N	Z
0	1	0	0	0	0					
5	5	0	1	1	0					
5	5	1	0	0	1					
8	1	0	0	1	0					
7	1	0	0	1	0					

13. What is the essential difference between a latch and a flip-flop?
   A. A latch is combinational logic, but a flip-flop is sequential.
   B. A latch is sequential logic, but a flip-flop is combinational.
   C. A latch can change state multiple times during a clock pulse, but a flip-flop will never change state more than once per clock pulse.
   D. A latch will never change state more than once per clock pulse, but a flip-flop can change state multiple times during a clock pulse.
   E. Latches are used to build counters, but flip-flops are used to build ALUs.

14. How do you keep a D flip-flop from changing state when it receives a clock pulse?
    A. Connect the D input to ground.
    B. Connect the Q output to ground.
    C. Connect the Q output to the D input.
    D. Connect the Clock input to the D output.
    E. Connect the Q output to an XOR gate.

15. How can you make a D flip-flop toggle when it receives a clock pulse?
    A. Connect the D input to the inverted value of the Q output.
    B. XOR the Clock and the D inputs, and connect the result to Q.
    C. Disable the Q output.
    D. Disable the D input.
    E. Connect a toggle gate to the Clock output.

16. How many flip-flops would it take to build a binary counter that divides a 1024 Hz clock to produce a 1 Hz clock?
    A. 1
    B. 10
    C. 26
    D. 48
    E. 1024

17. On the back of this sheet, draw a state diagram (circles and arcs) for a FSM that has four states named State_0, State_1, State_2, and State_3. If an external input named "Up" is true, the FSM goes to the next state in the sequence listed in the first sentence (*i.e.*, State_0 to State_1, State_1 to State_2, etc.) If an external input named "Dn" is true, the FSM switches to the next state in the reverse order from that listed in the first sentence (*i.e.*, State_0 to State_3, State_1 to State_0, etc.). If an external input named "Rst" is true, the FSM goes to State_0 regardless of whether "Up" or "Dn" is true. If Rst is false and both Up and Dn are true, the FSM stays in the same state. *There are four external outputs, with names matching the state names, <u>one</u> of which is true depending on which of the four states the FSM is in at any time.* Label all circles and arcs appropriately.

18. Assume two flip-flops named S1 and S0 are used to encode the four states of the FSM in Question 17 in the "natural" way. That is, both flip-flops are off in State_0, both are on in State_3, etc. Complete the indicated rows of the State Table for the FSM:

External Inputs			Present State		Next State		External Outputs			
Rst	Up	Dn	S1	S0	S1	S0	State_0	State_1	State_2	State_3
0	0	0	1	1						
1	1	1	1	0						
0	1	0	1	1						
0	0	1	1	1						

19. What do the S1 and S0 values in the Present State part of the state table represent?
    A. The D inputs to the flip-flops.
    B. The Clock inputs to the flip-flops.
    C. The Q outputs of the flip-flops.
    D. The values of the Up and Dn inputs.
    E. They tell whether the LEDs are on or off.

20. What problem is solved by using tristate buffers?
    A. They eliminate propagation delays.
    B. They allow the inputs of multiple gates to be connected together without causing fan-out problems.
    C. They allow XOR gates to toggle when their outputs change state.
    D. They convert the clock period into the corresponding frequency.
    E. They allow the outputs of multiple gates to be connected together provided no more than one tristate buffer is enabled at a time.