NOTE: It is my policy to give a failing grade in the course to any student who either gives or receives aid on any exam or quiz.

INSTRUCTIONS: Answer all arabic-numbered questions (1, 2, 3, …) on your Scantron answer sheet. Answer roman-numbered questions (I, II, III, …) on the backs of the question sheets. Use a pencil for all your answers. *Note:* The number in parentheses at the beginning of each question gives the relative weight for the question. The weights do not sum to 1.0

NO CALCULATORS

1. (0.05) The time it takes a gate to change state after its inputs change is called what?
   A. Modification time
   B. I/O time
   C. A race
   D. 3 picoseconds
   E. Propagation delay
2. (0.05) The number of wires going into a gate is called what?
   A. I/O Count
   B. Load factor
   C. Fan-in
   D. Gate output count
   E. Karnaugh Map
3. (0.05) How can you determine the fan-out of a gate?
   A. Look it up in the manufacturer's data sheet for the gate
   B. Count the number of wires going into the gate
   C. Count the number of wires going out of the gate
   D. Count the number of other gates to which the output is connected
   E. You can't
4. (0.05) Why is a GPA calculated to three decimal places instead of either two or four places?
   A. Because three places is easier to compute than four, and two places is too easy.
   B. Because there is a law that requires all GPAs to be calculated to two places, and Queens College wanted to do better than the law required.
   C. Because there is a law that requires all GPAs to be calculated to four places, but Queens College obtained an exemption from the law.
   D. Because three places is the minimum number needed to discriminate between minimally different sets of grades, and four places adds no more information than three.
   E. Because three places is a power of 2, but two and four are not.
5. (0.05) Convert 50 picoseconds to nanoseconds.
   A. 50,000 nanoseconds
   B. 0.020 nanoseconds
   C. 20,000 nanoseconds
   D. 0.00020 nanoseconds
   E. 0.050 nanoseconds
6. (0.05) Convert 50 nanoseconds to picoseconds.
   A. 50,000 picoseconds
   B. 0.020 picoseconds
   C. 20,000 picoseconds
   D. 0.00020 picoseconds
   E. 0.050 picoseconds
7. (0.05) What is the period of a 1KHz signal?
   A. 1 second
   B. 1 millisecond
   C. 1 microsecond
   D. 1 nanosecond
   E. 1 picosecond

8. (0.05) I am thinking of an integer between 1 and 64. How much uncertainty do you have about the value of the number?
   A. None
   B. Infinite
   C. 1 bit
   D. 6 bits
   E. 64 bits

9. (0.05) How many bytes are there in a 32 gigabyte memory?
   A. 32,768
   B. 32,768,768
   C. $2^7 * 2^{10}$
   D. $2^6 * 2^{20}$
   E. $2^5 * 2^{30}$

10. (0.05) 20% of the instructions in a program take 1 nsec to execute, 30% take 2 nsec to execute, and the rest take 3 nsec to execute. What is the average execution time per instruction for this program?
   A. 1.2 nsec
   B. 2.1 nsec
   C. 1.3 nsec
   D. 3.1 nsec
   E. 2.3 nsec

11. (0.05) A computer monitor has a display area of 2,048 * 1,024 pixels, and each pixel can display any one of 2^{24} colors. How many bits of memory would be required to store a single image for this monitor?
   A. $2^{11} * 2^{10} * 24$
   B. $2^{20} * 2^{10} * 2^{24}$
   C. $(2{,}048 + 1{,}024) * 2^{24}$
   D. $\log_2(3{,}024 * 2^{24})$
   E. $(2^{20} * 2^{10} * 2^{24}) / 2^3$

I. (0.10) Draw all the gates to implement an *unclocked R-S latch* on the back of one of the exam sheets. Label all inputs and outputs meaningfully.

II. (0.10) Draw all the gates to implement a *J-K Master Slave flip-flop* on the back of one of the exam sheets. Label all inputs and outputs meaningfully.

III. (0.10) Draw a *timing diagram* for a clocked D latch on the back of one of the exam sheets. Design your diagram so there are three clock pulses. Make the state of the latch false at the beginning. Make the D input false during the first two clock pulses, and make it true during the third one. Complete the rest of the diagram based on the requirements given above.

IV. (0.10) On the back of an exam sheet, draw a state diagram (circles and arcs) for a two-bit down counter with no external inputs and an external output named "Odd" that is true whenever the counter's numeric value is an odd number. Complete the state table for the counter below. *Extra Credit:* Draw a circuit that implements this Finite State Machine next to your state diagram.

Present State		**Next State**		**Flip-Flop Inputs**				**External Output**
S_1	**S_0**	**S_1**	**S_0**	**J_1**	**K_1**	**J_0**	**K_0**	**Odd**
0	**0**							
0	**1**							
1	**0**							
1	**1**							