

RDRAM). The MCH integrates AGTL+ termination resistors on all of the AGTL+ signals. The MCH supports 32-bit host addressing, allowing the processor to access the entire 4 GB of the MCH's memory address space. The MCH has an 8-deep In-Order Queue to support up to eight outstanding pipelined address requests on the host bus. Host initiated I/O cycles are positively decoded to AGP or MCH configuration space. Host-initiated I/O cycles are subtractively decoded to the hub interface. Host-initiated memory cycles are positively decoded to AGP or RDRAM and are again subtractively decoded to the hub interface. AGP semantic memory accesses initiated from AGP to DRAM are not snooped on the host bus. Memory accesses initiated from AGP using PCI semantics and from the hub interface to DRAM are snooped on the system bus. Memory accesses whose addresses lie within the AGP aperture are translated using the AGP address translation table, regardless of the originating interface.

RDRAM Interface

The MCH directly supports two channels of Direct RDRAM memory operating in lock-step using RSL technology. The MCH RDRAM channels run at 300 MHz, 400 MHz and 533 MHz and support 128-Mb and 256-/288-Mb technology RDRAM Direct devices. These 128-Mb and 256-/288-Mb RDRAMs use page sizes of 1 KB, while 256-/288-Mb devices may also be configured to use 2 KB pages. For 82850 MCH and 82850E MCH PC800 RDRAM a maximum of 64 RDRAM devices are supported on the paired channels without external logic. For 82850E MCH PC1066 RDRAM a maximum of 24 RDRAM devices are supported on the paired channels. The following tables show the maximum RDRAM array size and the minimum increment size for the various RDRAM densities supported.

Table 1. RDRAM* Densities Supported

| MCH Stepping | Device Tech | Device Quantity | No. of Banks | Page Size |
|--------------|--------------|-----------------|--------------|-----------|
| A2, A3 | 128/144 Mbit | 4,8,16 | 16d | 1 KB |
| A2, A3 | 128/144 Mbit | 4,8,16 | 2x16d | 1 KB |
| A3 | 288 Mbit | 4,8,16 | 16d | 2 KB |
| A3 | 256/288 Mbit | 2,4,8,16 | 2x16d | 2 KB |
| A3 | 256/288 Mbit | 4,8,16 | 32s | 2 KB |

Table 2. Maximum RDRAM* Array Size, Minimum Increment Size

| RDRAM* Technology | Directly Supported | | |
|-------------------|--------------------|-----------------------|-----------------------|
| | Increments | Maximum 400 MHz RDRAM | Maximum 533 MHz RDRAM |
| 128 Mb | 32 MB | 1 GB | 1 GB |
| 256/288 Mb | 64 MB | 2 GB | 1.5 GB |